

FIG. 1

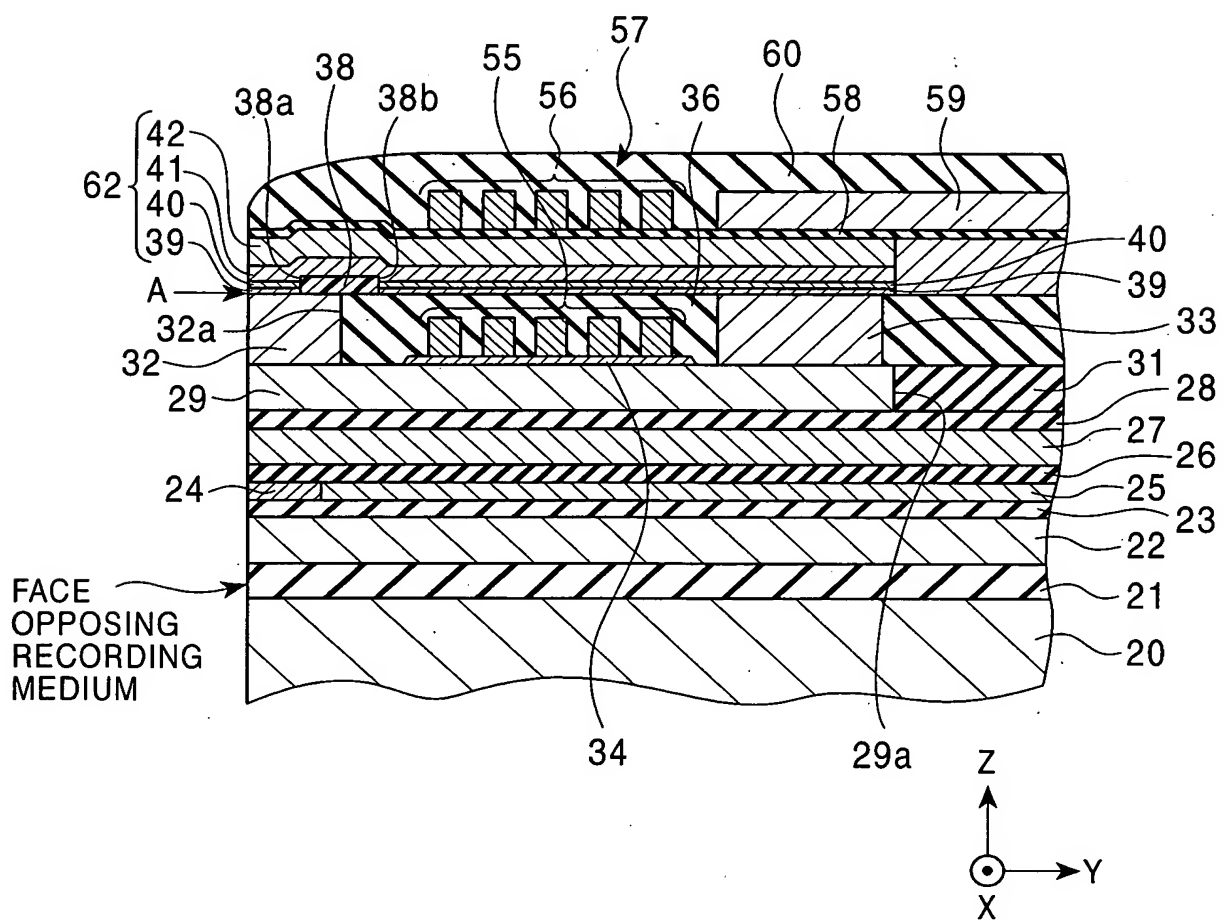


FIG. 2

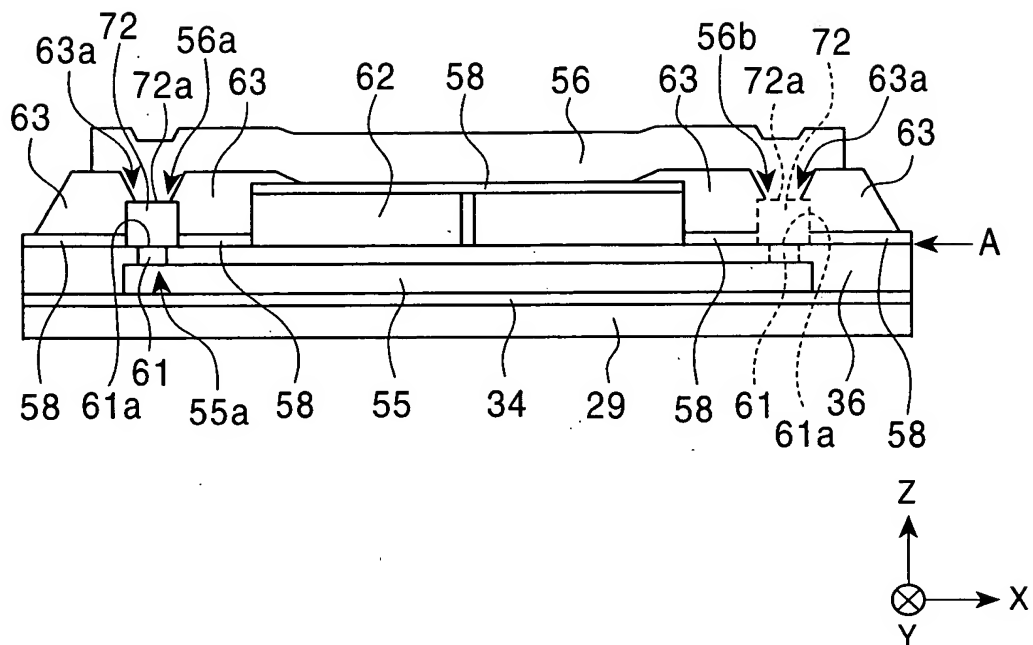


FIG. 3

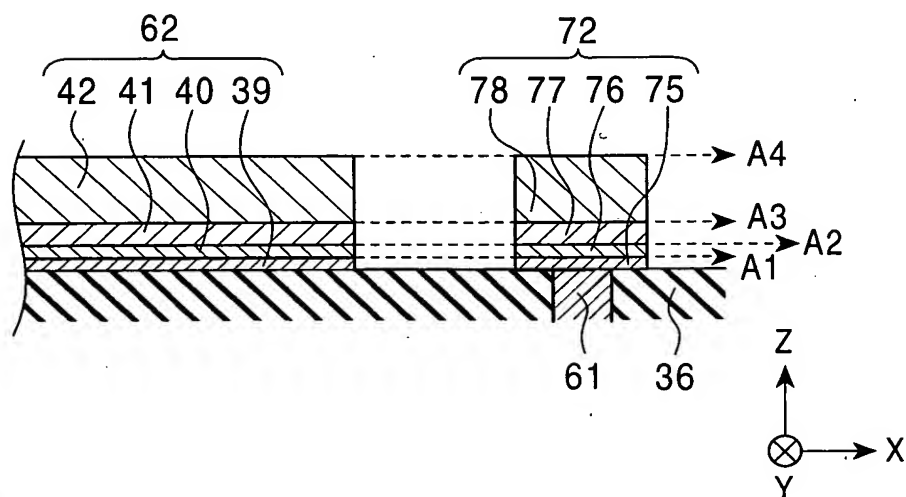
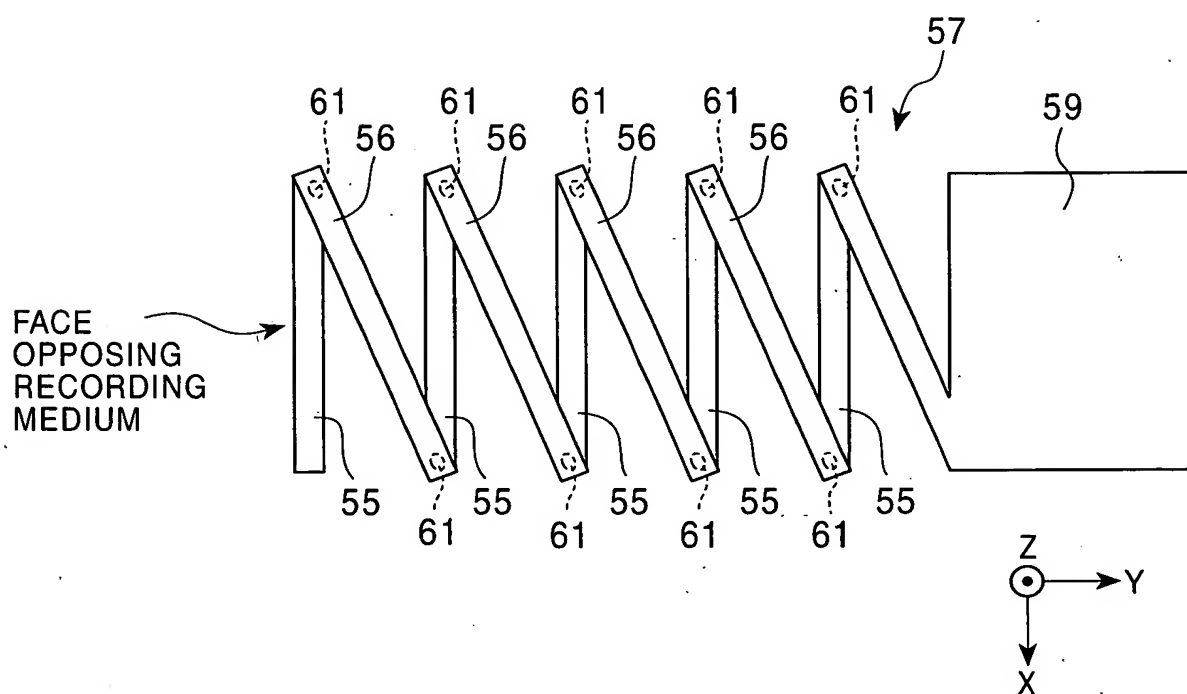


FIG. 4



[illegible]

FIG. 6

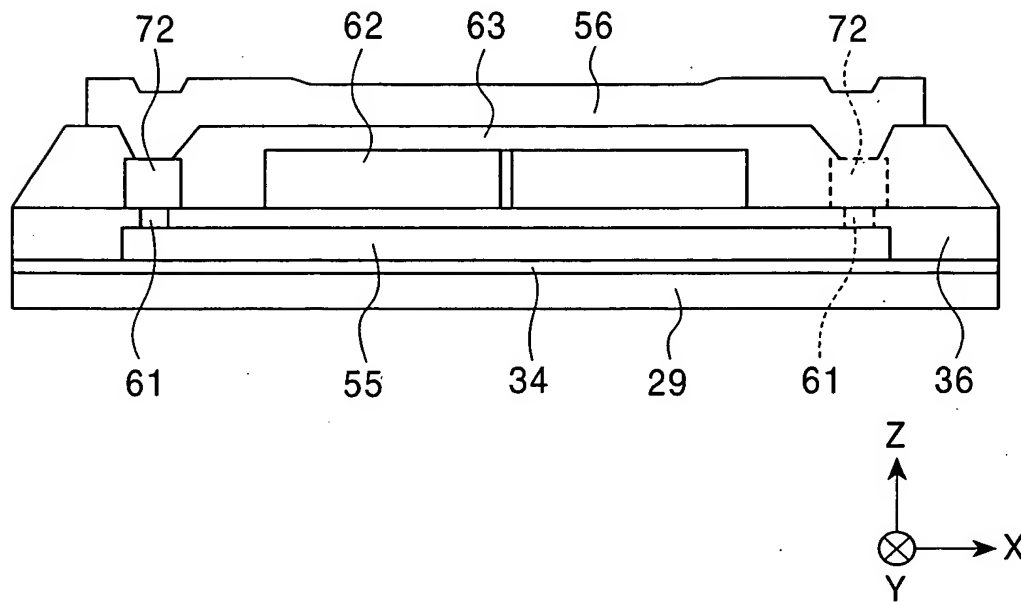


FIG. 7

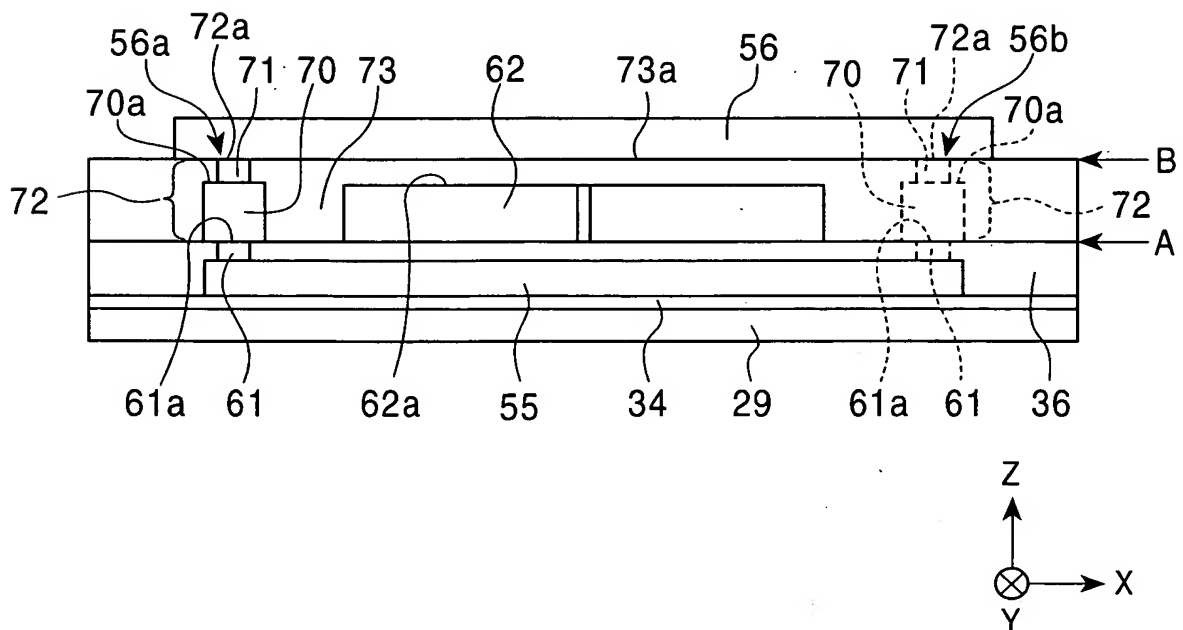
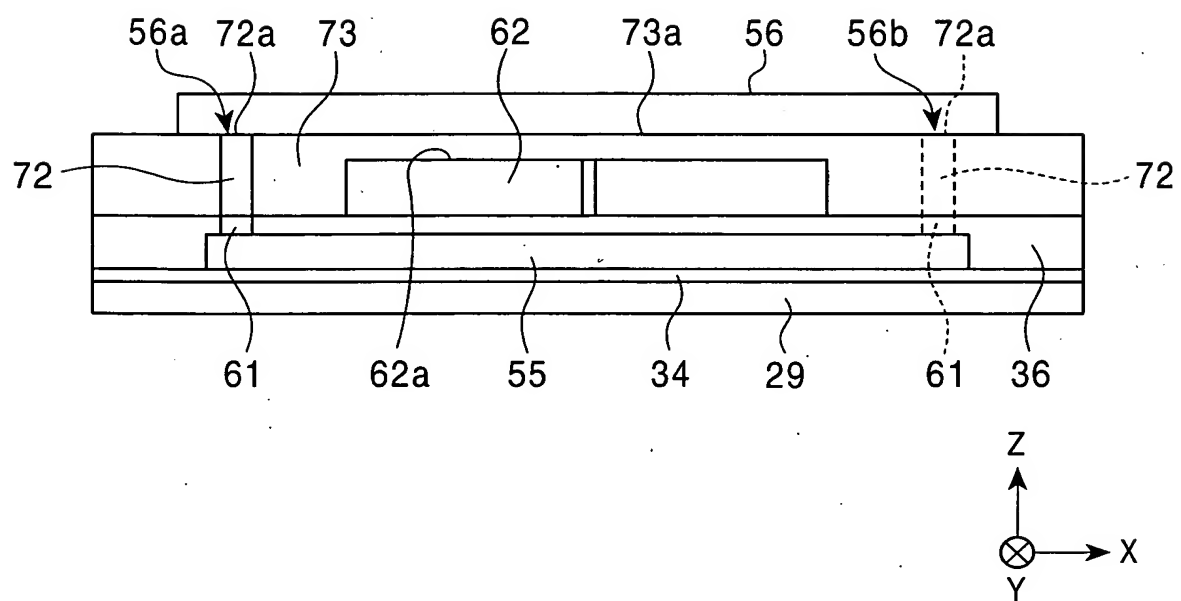


FIG. 8



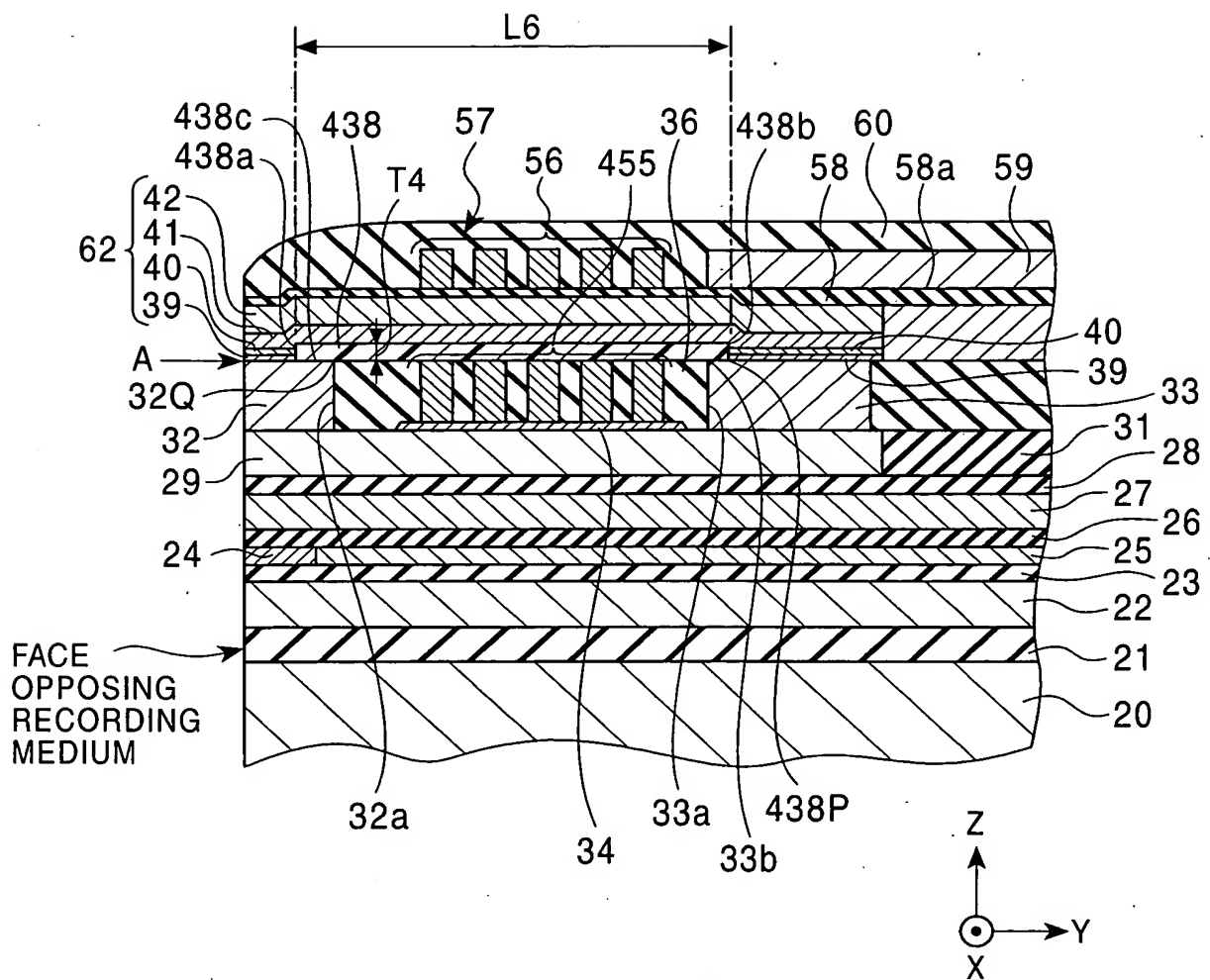


FIG. 10

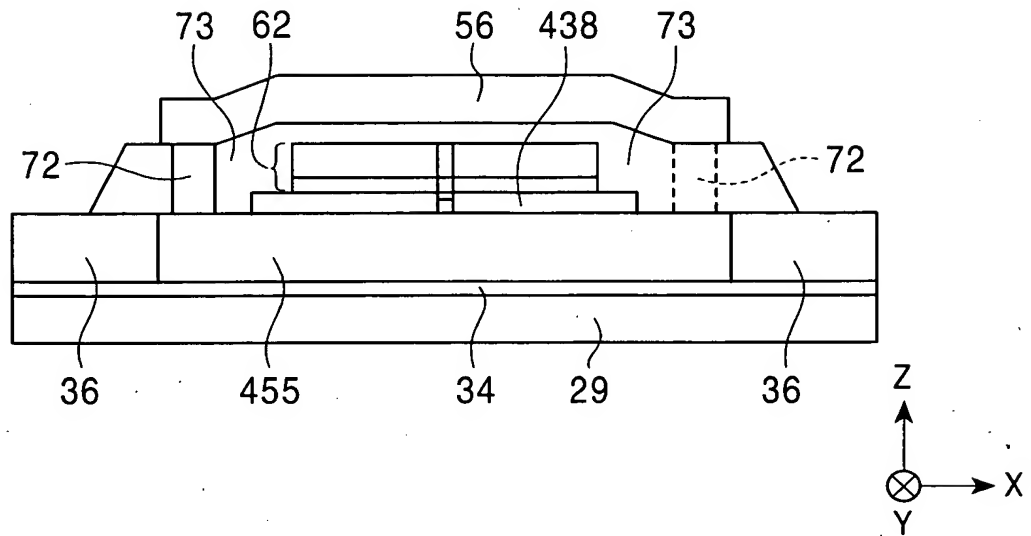


FIG. 11

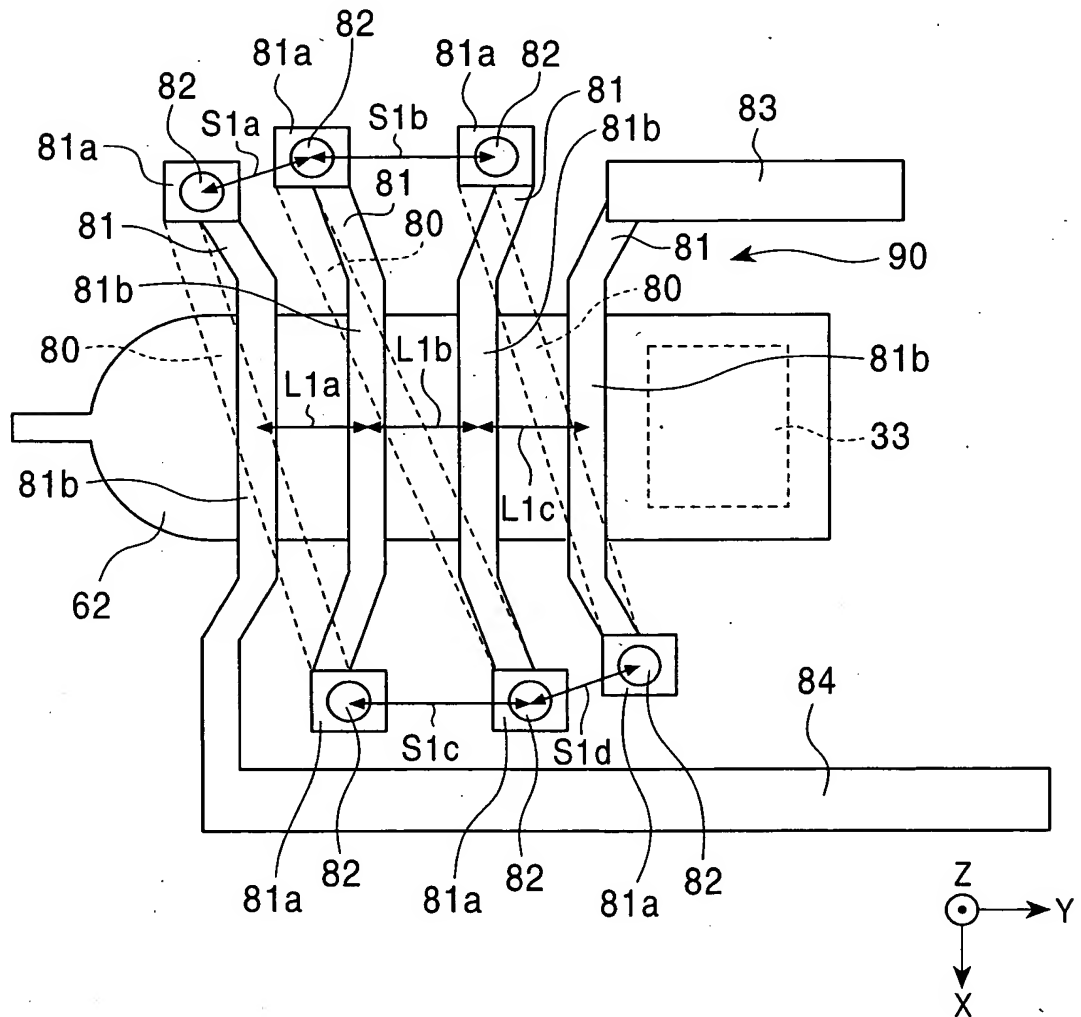




FIG. 12

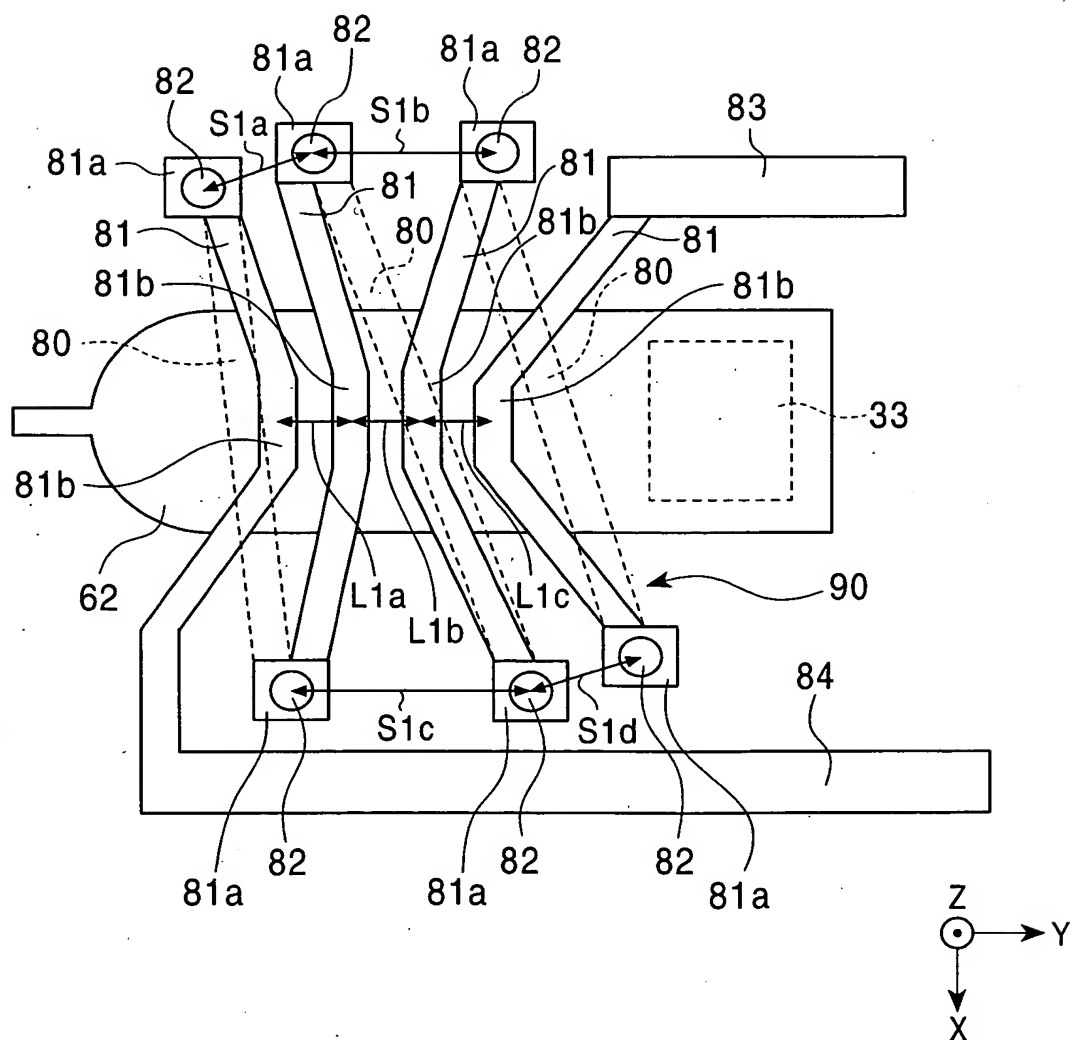


FIG. 13

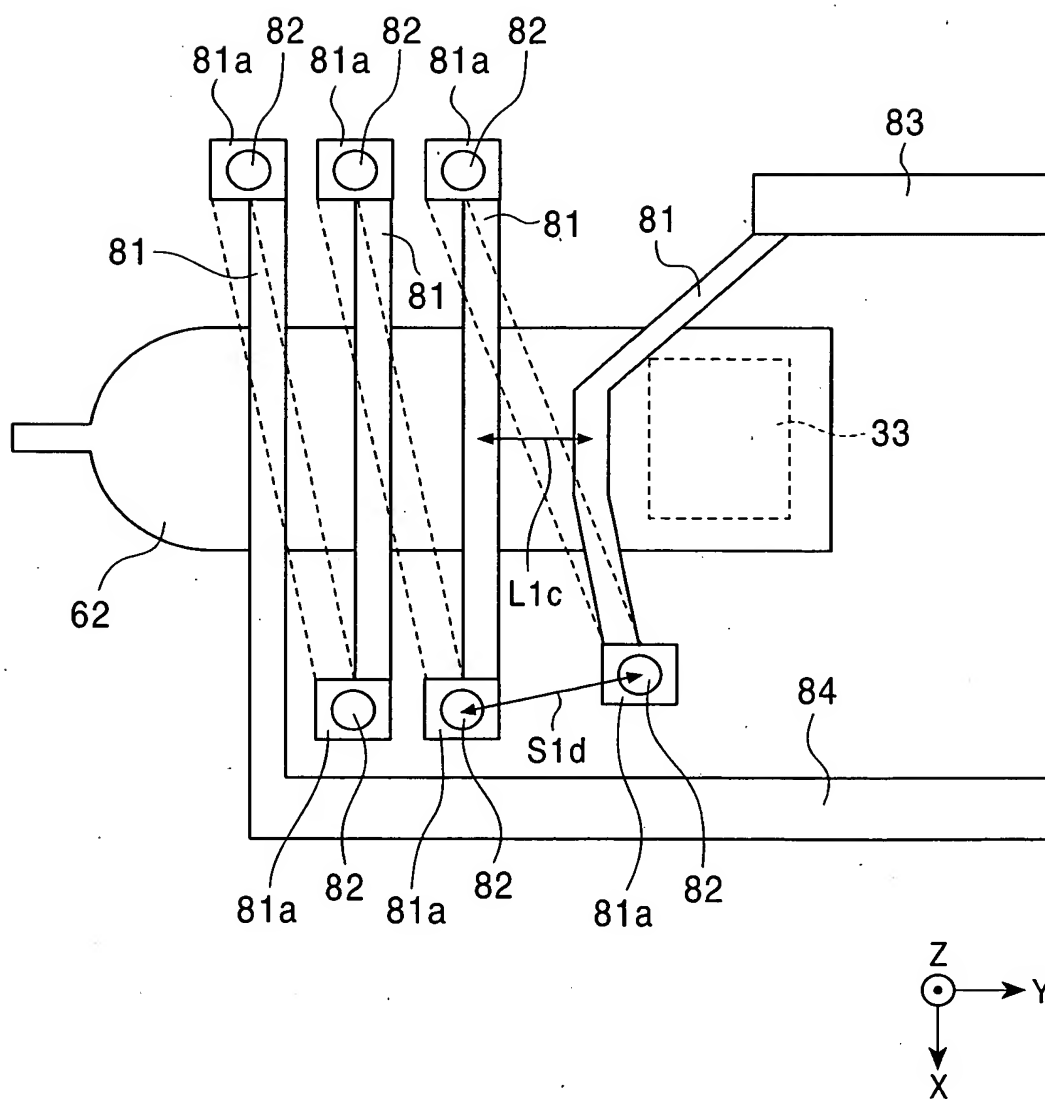


FIG. 14

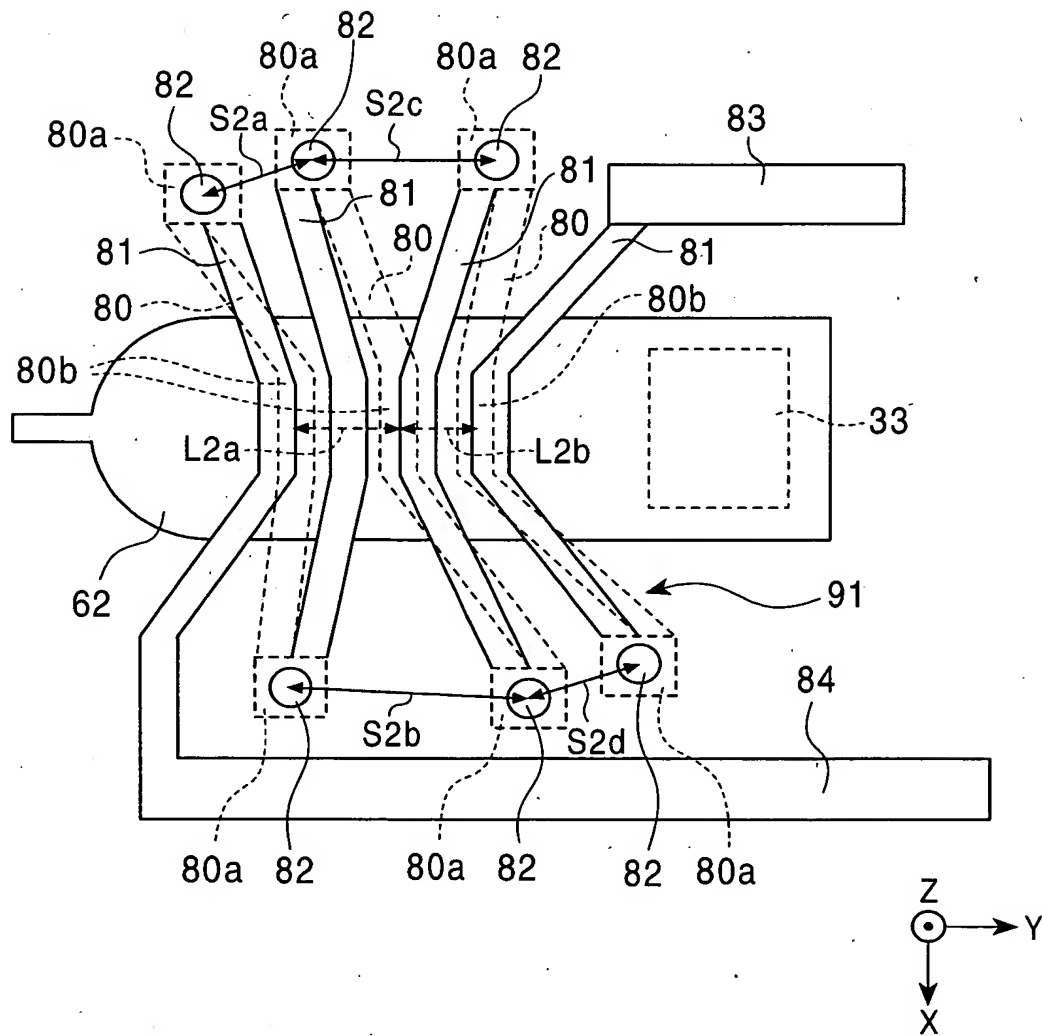
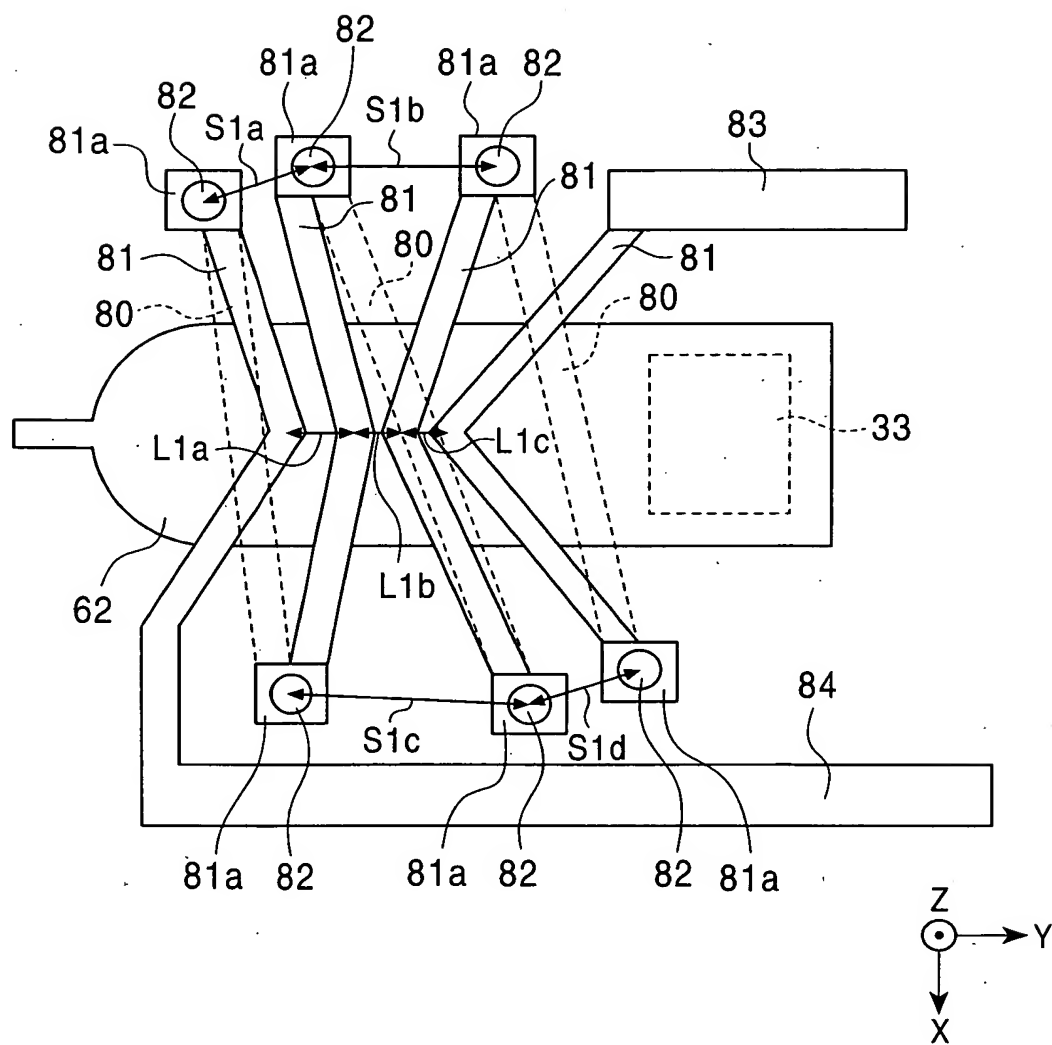
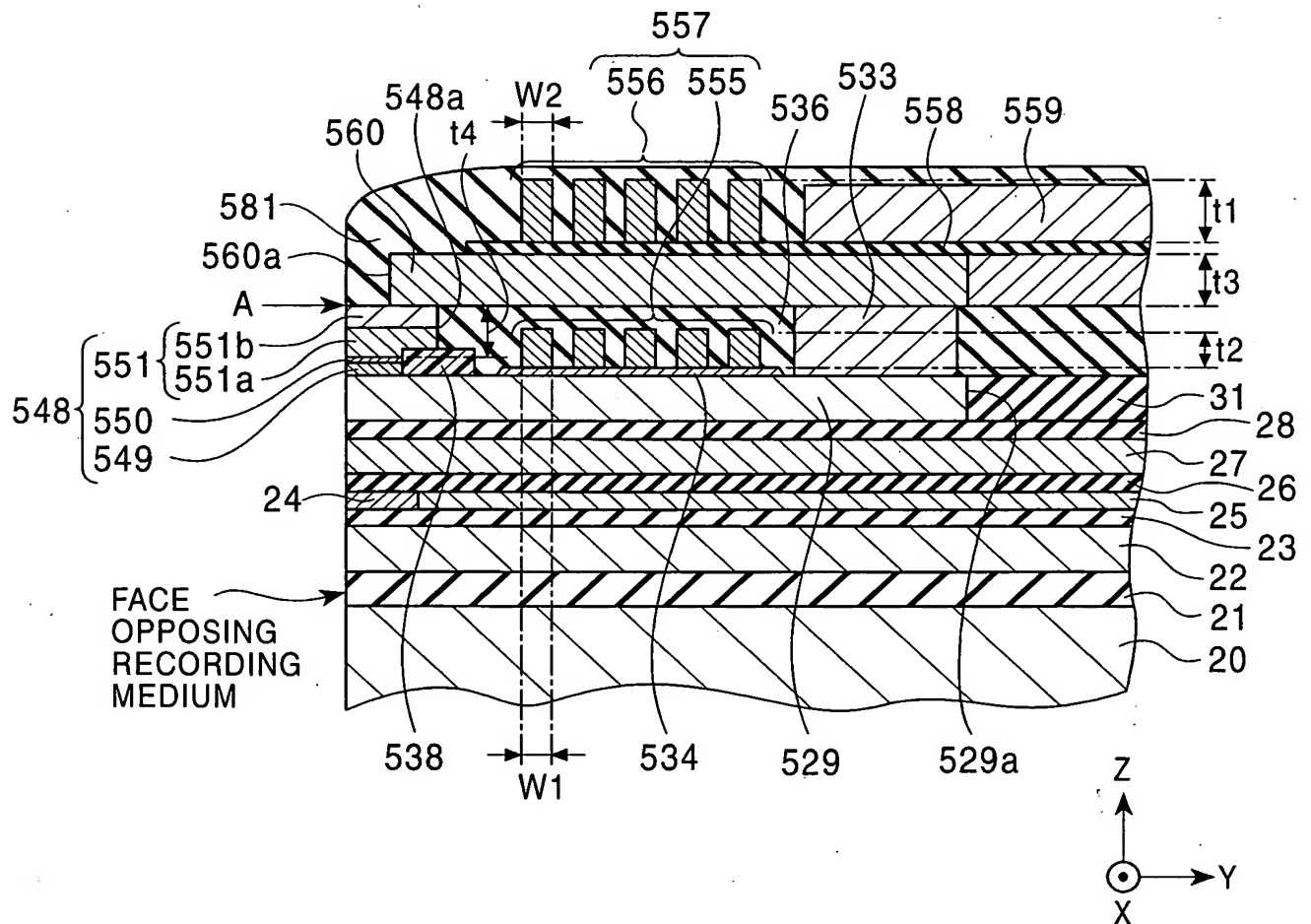


FIG. 15





This cross-sectional diagram shows the internal layers of the device. The substrate consists of a base layer 529, followed by a stack of layers 558, 561, 555, and 555a. On top of these is a thin layer 534, which contains regions 550, 549, and 551. Above the substrate are several conductive layers: 557, 556, 558, and 560. These layers are patterned into various shapes, including rectangular blocks 563 and 563a, and narrow strips 572 and 572a. Some features like 561a and 561b are shown as dashed outlines. A dimension line labeled Tw indicates the thickness of a specific layer. A coordinate system at the bottom right shows Z pointing up, X pointing right, and Y pointing out of the page.

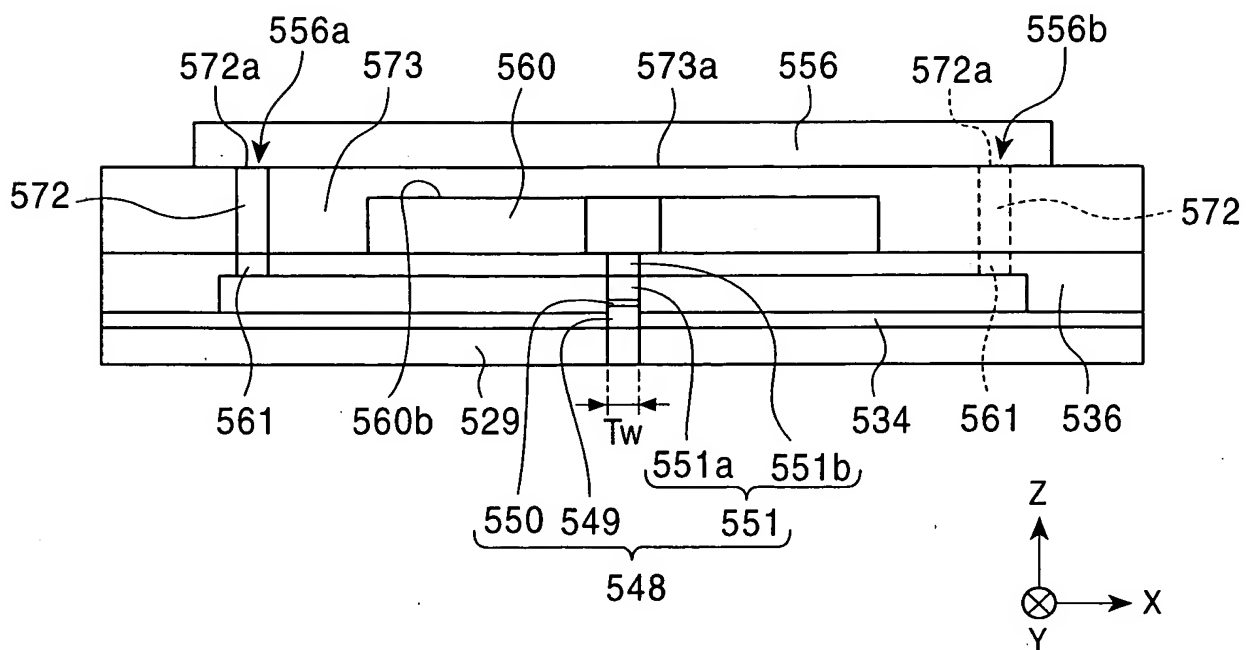


FIG. 20

